IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device having a multilayer wiring structure, comprising

a bypass capacitor;

a first power line connected to [[a]] one terminal of said bypass capacitor;

a second power line connected to another terminal of said bypass capacitor;

a ~~second~~ third power line from which a part corresponding to a position of said bypass capacitor is removed; [[and]]

a fourth power line from which a part corresponding to the position of said bypass capacitor is removed;

a first contact for connecting said first power line and said ~~second~~ third power line; and

a second contact for connecting said second power line and said fourth power line.

2. (Original) The semiconductor device according to claim 1, wherein a plurality of said contacts is provided.

3. (Original) The semiconductor device according to claim 1, wherein said contact is attached to an end of said second power line.

4. (Original) The semiconductor device according to claim 1, wherein said contact is made wider than said first power line and said second power line.

5. (Original) The semiconductor device according to claim 1, wherein said bypass capacitor is installed close to a circuit which is supplied with power.

6. (Original) The semiconductor device according to claim 5, wherein said circuit is an I/O cell installed around a semiconductor tip.

7. (Original) The semiconductor device according to claim 1, wherein:

said bypass capacitor is a transistor comprising:

a gate electrode formed on a semiconductor substrate through a gate insulating film; and

source/drain regions formed on the semiconductor substrate with said gate electrode inserted therebetween; and

said first power line is connected to one of said source/drain regions and said gate electrode of said transistor.

8. (Original) The semiconductor device according to claim 1, wherein said second power line is installed in an upper wiring layer than said first power line.